BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Capacitors, Dynamic Random Access Memory (DRAM) Circuitry, Methods Of Forming Capacitors, And Methods Of Forming DRAM Circuitry

* * * * *

INVENTORS

Martin Ceredig Roberts
Christophe Pierrat

ATTORNEY'S DOCKET NO. MI22-924

CAPACITORS, DYNAMIC RANDOM ACCESS MEMORY (DRAM) CIRCUITRY, METHODS OF FORMING CAPACITORS, AND METHODS OF FORMING DRAM CIRCUITRY

TECHNICAL FIELD

This invention relates to capacitors, dynamic random access memory (DRAM) circuitry, to methods of forming capacitors, and to methods of forming DRAM circuitry.

BACKGROUND OF THE INVENTION

As integrated circuitry increases in density, there is a continuing challenge to maintain sufficiently high storage capacitances for storage capacitors despite decreasing circuitry dimensions. In particular, as DRAMs increase in memory cell density, there is a continuing challenge to maintain sufficiently high storage capacitance despite decreasing cell areas. Additionally, there is a continuing goal to further decrease cell areas. One principle way of increasing cell capacitance is through cell structure techniques. Such techniques include three-dimensional cell capacitors, such as trench or stacked capacitors.

This invention arose out of concerns associated with improving capacitor storage capabilities through improved structures and formation techniques.

SUMMARY OF THE INVENTION

Capacitors, DRAM circuitry, and methods of forming the same are described. In one embodiment, a capacitor comprises a first container which is joined with a substrate node location and has an opening defining a first interior area. A second container is joined with the node location and has an opening defining a second interior area. The areas are spaced apart from one another in a non-overlapping relationship. A dielectric layer and a conductive capacitor electrode layer are disposed operably proximate the first and second containers. In another embodiment, the first and second containers are generally elongate and extend away from the node location along respective first and second central axes. The axes are different and spaced apart from one another. In yet another embodiment, a conductive layer of material is disposed over and in electrical communication with a substrate node location. The layer of material has an outer surface with a first region and a second region spaced apart from the first region. A first container is formed over and in electrical communication with the first region and a second container is formed over and in electrical communication with the second region. In yet another embodiment, the first and second containers define container volumes which are discrete and separated from one another.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic side sectional view of a semiconductor wafer fragment in process in accordance with one or more embodiments of the present invention, and is taken along line 1-1 in Fig. 11.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 7.

Fig. 9 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 8.

Fig. 10 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 9.

Fig. 11 is a top plan view of a layout of a portion of a semiconductor substrate which has been processed in accordance with one or more embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment is shown generally at 20 and includes semiconductive substrate 22. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Isolation regions 24 are provided and comprise, typically, an oxide material. Regions 24 can be formed through any suitable technique such as shallow trench isolation techniques. A plurality of conductive lines 26, 28, 30, and 32 are formed over substrate 22 and include, respectively, a gate oxide layer (not specifically shown), a polysilicon layer 34, a silicide layer 36, an insulative cap 38 and sidewall

spacers 40. Of course, other conductive line constructions could be used, with lines 26-32 constituting but one example. In the illustrated example, conductive lines 26, 28, 30, and 32 comprise word lines for dynamic random access memory (DRAM) circuitry. Active areas 42 comprising node locations with which electrical communication is desired are defined intermediate isolation regions 24.

Referring to Fig. 2, an insulative layer 44, e.g. BPSG, is formed over substrate 22 and planarized. Openings 46 are etched or otherwise formed into layer 44 sufficiently to expose active areas 42. Such openings can be, and preferably are formed over areas where both storage capacitors and bit lines are to establish electrical communication with respective associated active areas. The openings are filled with conductive material 48, which can be subsequently etched back for isolation over the individual respective active areas. An exemplary material for conductive material 48 is conductively doped polysilicon.

Referring to Fig. 3, a layer 50 is formed over substrate 22 and comprises an insulative material such as BPSG which can be subsequently planarized.

Referring to Fig. 4, openings 52 are etched through layer 50 sufficiently to expose conductive material 48. Additional conductive material 54 is formed over and in electrical communication with conductive material 48 and is isolated within openings 52. An exemplary material for conductive material 54 is conductively doped

polysilicon. Openings 52 are formed to coincide with node locations over which storage capacitors are to be formed.

Referring to Fig. 5, an insulative material layer 56, e.g. BPSG, is formed over substrate 22 and subsequently planarized.

Referring to Fig. 6, a patterned masking layer 58, e.g. photoresist, is formed over substrate 22 and pairs of openings 60 (formed over conductive lines 26, 28) and 62 (formed over conductive lines 30, 32) are formed first within masking layer 58, and subsequently etched into layer 56. In a preferred embodiment, improved patterning resolution of the openings can be achieved through utilization of alternating phase shift contact techniques. In alternating phase shift contact techniques, immediately adjacent cell areas are provided or fabricated with their light during exposure exactly 180° out of phase. Such can be implemented by using a special mask or reticle. With a special mask or reticle, the glass of the reticle at adjacent openings is provided alternatingly, such that a cut is made into the glass portion of the mask a suitable distance such that the light shifts 180° out of phase. Such can provide better lithographic resolution between adjacent devices.

Referring to Fig. 7, a conductive material layer 64 is formed over substrate 22 and within openings 60, 62. An exemplary material comprises polysilicon.

Referring to Fig. 8, material of layer 64 is removed from over selected portions of layer 56 as by chemical-mechanical polishing to isolate conductive material within openings 60, 62. Such effectively

forms capacitor containers as will become apparent below. At this point in processing, additional processing can take place to provide roughened surfaces over the interior of conductive material 64 which can increase the capacitance of the resultant capacitors. Such can take place through known techniques for depositing hemispherical grain polysilicon (HSG) or cylindrical grain polysilicon (CSG).

Referring to Fig. 9, material of layer 56 is etched back or otherwise removed from over substrate 22 and effectively defines individual containers 66, 68, 70, and 72. In the illustrated example, two containers are formed for each node location 42. For example, containers 66, 68 comprise first and second containers respectively, which are joined with the leftmost node location 42. Similarly, containers 70, 72 comprise third and fourth containers which are joined with the rightmost node location 42. Each container includes a respective opening 66a, 68a, 70a, and 72a away from the node location with which it is associated and which defines an interior area. The interior areas for each container are spaced apart from one another in a non-overlapping relationship.

In this example, containers 66-72 are generally elongate and extend along respective individual central axes (indicated by the dashed lines), and away from the node locations with which each joins. Preferably, the central axes are spaced apart from, and generally parallel with one another. In a preferred embodiment, openings 66a, 68a, 70a, and 72a are generally circular in shape and the

containers are generally tubular or cylindrical, i.e. generally circular in transverse cross section, in construction.

Alternately considered, conductive material 54 includes an outer surface with first and second regions 74, 76 respectively. The regions are preferably spaced apart from one another, and individual containers 66, 68 are respectively joined with individual first and second regions 74, 76 respectively. The same can be said for containers 70, 72 with respect to regions 74, 76 provided by their associated conductive material 54.

Further alternately considered, formation of containers 66-72 results in containers which define volumes which are substantially the same in magnitude, and which are discrete and separated from one another.

Referring to Fig. 10, a dielectric layer 78 is formed operably proximate each container and a conductive capacitor electrode layer 80 is formed thereover. Collectively, containers 66, 68, dielectric layer 78, and electrode layer 80 provide one storage capacitor for a DRAM array and containers 70, 72, dielectric layer 78, and electrode layer 80 provide another storage capacitor for the DRAM array. In a preferred embodiment, the storage capacitors comprise only two conductive capacitor electrodes separated by a dielectric region.

Referring to Fig. 11, a circuit layout is shown which depicts active areas 82 and individual containers which appear as generally circular regions disposed over or proximate active areas 82. Individual storage capacitors are shown by the dashed lines 84, 86. In this layout, word

lines (WL) and digit lines (DL) would extend in the indicated respective directions and generally within the areas occupied by the respective arrows. In a reduction-to-practice example, capacitor containers were fabricated having dimensions d_1 and d_2 as shown, with d_1 being equal to about 0.67 micron, and d_2 being equal to about 0.27 micron. Such dimensions can constitute an increase in capacitance from between about 11 percent to 15 percent over conventional DRAM constructions.

Advantages of the present invention can include an increase or gain in capacitance over previous structures without an undesirable associated increase in consumed wafer area.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.